

FIG. 1

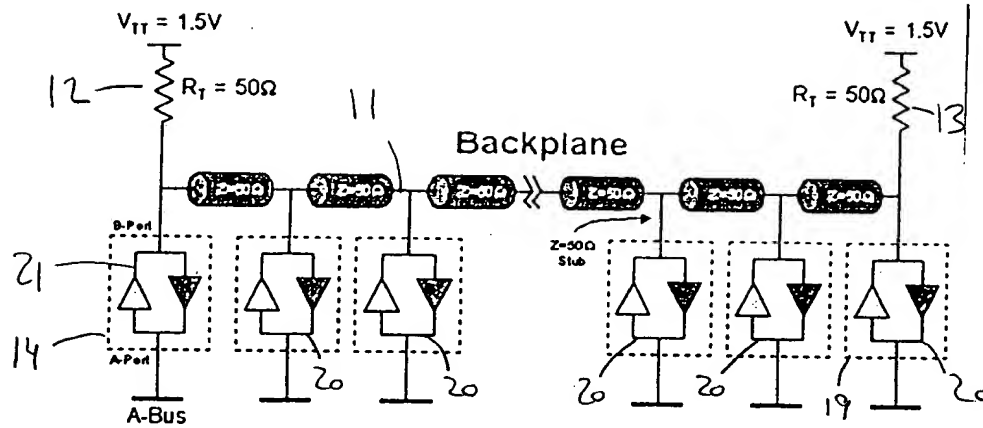


FIG. 2

Clock Path Timing

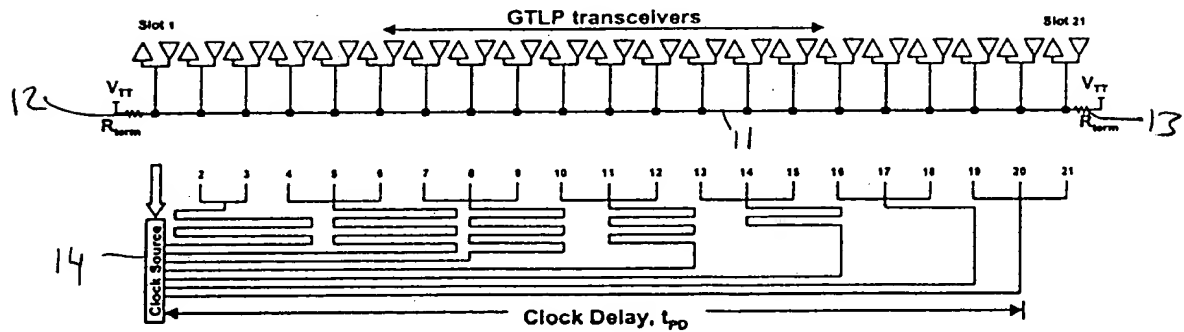


FIG. 3

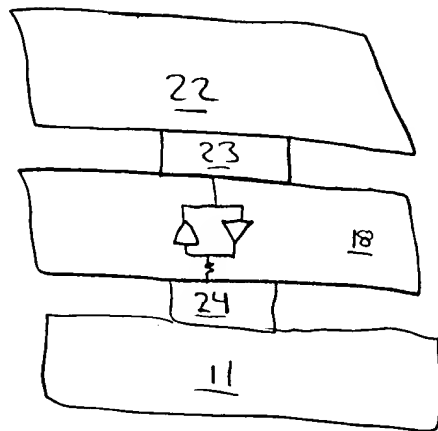


FIG. 4

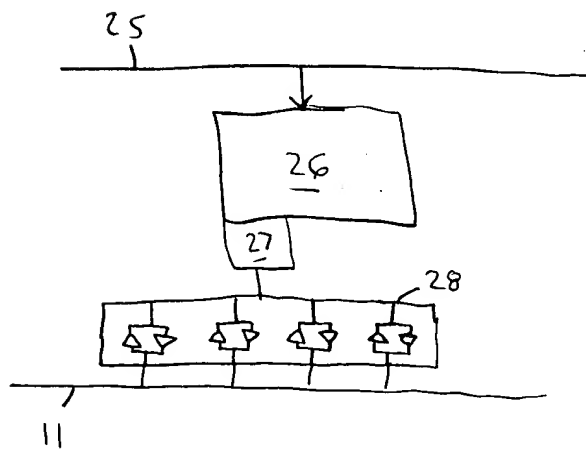


FIG. 5

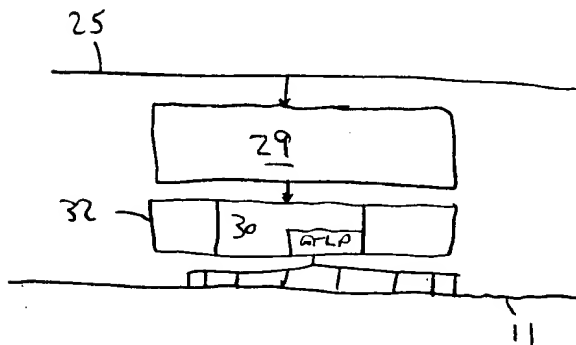


FIG. 6